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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,076	09/19/2001	Eiji Sakagami	214019US2	9771

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[REDACTED] ART UNIT [REDACTED] PAPER NUMBER

2814

DATE MAILED: 11/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/955,076	SAKAGAMI, EIJI
Examiner	Art Unit	
Howard Weiss	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
 THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 06 September 2002.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 7-21 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-6 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) 1-21 are subject to restriction and/or election requirement

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

- 11) The proposed drawing correction filed on 06 September 2002 is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) Interview Summary (PTO-413) Paper No(s) _____
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other _____

Attorney's Docket Number: 214019US2

Filing Date: 9/19/01

Continuing Data: none

Claimed Foreign Priority Date: 9/21/00 (JPX)

Applicant(s): Sakagami

Examiner: Howard Weiss

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 9/6/02 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura et al. (U.S. Patent No. 6,255,166) and Inoue (U.S. Patent No. 5,559,048).

Ogura et al. show most aspects of the instant invention (e.g. Figure 1) including:

- ✓ a semiconductor substrate **10**
- ✓ a first transistor used as a cell transistor including a first gate insulating film **132** and a first gate electrode **142**
- ✓ a second transistor used as a selection transistor including a second gate insulating film **131** and a second gate electrode **141**

- said first gate insulating film comprising a charge storage layer **132b** made of silicon nitride or tantalum oxide with top **132c** and bottom **132a** layers of silicon oxide and said charge storage layer existing only below the first gate electrode in an element region

Ogura et al. do not show the first and second transistor isolated by a trench and said charge storage layer restricted from an element isolation region. Inoue teach (e.g. Figure 8A) to isolate memory cells with trench isolations **108** in element isolation regions **107** with the charge storage layer **103/106** restricted from said element isolation regions to prevent leakage current flow (Column 9 Lines 36 to 52). It would have been obvious to a person of ordinary skill in the art at the time of invention to isolate memory cells with trench isolations in element isolation regions with the charge storage layer restricted from said element isolation region as taught by Inoue in the device of Ogura et al. to prevent leakage current flow.

4. Claims 2, 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura et al. and Inoue, as applied to Claim 1 above, and further in view of Reisinger.

Ogura et al. and Inoue show most aspects of the instant invention (Paragraph 3) except for the thickness ranges and that the thickness of the bottom oxide layer is smaller than the top oxide layer. Reisinger teaches (e.g. Figure 1 and Column 5 Lines 45 to 56) to form a triple layer gate insulating layer **5** with the thicknesses within the claimed ranges and with the thickness of the bottom oxide layer **51** is smaller than the top oxide layer **53** to increase storage density and data retention (Column 2 Lines 7 to 12). It would have been obvious to a person of ordinary skill in the art at the time of invention to form a triple layer gate insulating layer with the thicknesses within the claimed ranges and with the thickness of the bottom oxide layer is smaller than the top oxide layer as taught by Reisinger in the device of Ogura et al. and Inoue to increase storage density and data retention.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura et al., Inoue and Reisinger, as applied to Claim 1 above, and further in view of Agarwal et al. (U.S. Patent No. 6,201,276)

Ogura et al., Inoue and Reisinger disclose the claimed invention (Paragraph 4) except that the charge storage layer comprising either a silicon nitride or a tantalum oxide film instead of either a strontium titanate or a barium strontium titanate film. Agarwal et al. teach (Column 4 Lines 33 to 36) that either a strontium titanate or a barium strontium titanate film are equivalent structure known in the art. Therefore, because these charge storage films were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute either silicon nitride or tantalum oxide for strontium titanate or barium strontium titanate.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura et al. and Inoue, as applied to Claim 1 above, and further in view of Fang (U.S. Patent No. 6,023,085).

Ogura et al. and Inoue show most aspects of the instant invention (Paragraph 3) except for the first peripheral transistor consisting of a third gate insulating film and a third gate electrode and a second peripheral transistor consisting of a fourth gate insulating film and a fourth gate electrode and the thicknesses of the third and fourth gate insulating film being different. Fang teaches (e.g. Figure 9H) to have peripheral transistors **332, 342** with gate electrodes **338** and gate insulating films **337,336** of different thicknesses to improve performance and reliability while simplifying manufacture (Column 2 Lines 51 to 54). It would have been obvious to a person of ordinary skill in the art at the time of invention to have peripheral transistors with gate electrodes and gate insulating films of different thicknesses as taught by Fang in the device of Ogura et al. and Inoue to improve performance and reliability while simplifying manufacture.

Response to Arguments

7. The Applicant's arguments filed 9/6/02 have been fully considered but they are not persuasive. The Applicant states that Ogura et al. do not disclose or suggest a charge storage layer existing only below a first gate electrode and that Inoue does not show the charge storage layer restricted from the element isolation region. In reference to the charge storage layer existing only below a first gate electrode, Figure 1 of Ogura et al. specifically shows the charge storage layer **132b** existing only below a first gate electrode **G2**. In reference to the charge storage layer restricted from the element isolation region, Figure 8A of Inoue shows an embodiment with the charge storage layer **103/106** restricted from the element isolation region **107**. In view of these reasons and those set forth in the present office action, the rejections of the stated claims stand.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lin et al. (U.S. Patent No. 6,166,410) show the use of trench isolation in a MONOS cell.
9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **-7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications. The official TC2800 Before-Final, **(703) 872-9318**, and After-Final, **(703)-872-9319** Fax numbers will provide the fax sender with an auto-reply fax verifying receipt of their fax by the USPTO.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard Weiss at **(703) 308-4840** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via **Howard.Weiss@uspto.gov**.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 Receptionist at **(703) 308-0956**.

12. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/ 324,326	thru 11/6/02
Other Documentation: none	
Electronic Database(s): EAST	thru 11/6/02

HW/hw
6 November 2002

Howard Weiss
Examiner
Art Unit 2814

SUPERVISORY PATENT EXAMINER